Internship on Xilinx SoC Design Flow (30 hours)

Start date: 15th July 2024

Description:
Sandeepani offers Internship Program for students currently doing their B.E/B.Tech, M.E./M.Tech in Electronics/Instrumentation/Electrical/Telecommunication. This program is specifically designed with an objective to spark an interest in Digital System Design and Embedded System Design using Xilinx tools. The participants will get an opportunity to work on a project during the course.

Key takeaways:
- Introduction to Digital VLSI design flow – ASIC/FPGA/SoC Design Flow
- Verilog HDL language constructs
- Modelling Digital Circuits using Verilog HDL
- Functional simulation – Verilog Test Benches
- Coding For Synthesis, Verilog HDL coding Guidelines
- FPGA Design Flow – Xilinx Vivado tool Flow, RTL Analysis, Synthesis, Implementation, Bitstream Generation, Hardware Implementation on remote FPGA board
- Introduction to Zynq SoC Architecture
- Embedded System Design Flow using Xilinx Vitis
- Extend the hardware system with Xilinx provided peripherals

Eligibility criteria:
- Pursuing UG/PG/Research, Graduate/Post Graduate Student, Faculty, Working professional

Tools/Hardware/Software:
- Vivado, Vitis, Zynq-7000 SoC board

Key topics covered:
- Overview of Digital Electronics concepts – combinational and sequential circuits
- Introduction to Verilog HDL
- Introduction to Data flow modelling, Structural modelling and Behavioural modelling
- Writing Test Bench in Verilog HDL – Test Bench for Combinational and Sequential Logic
- Finite State Machine – Moore and Mealy FSM – FSM Coding Techniques
- HDL Coding Guidelines
- Simulation-Synthesis mismatch
- Introduction to FPGA Design Flow, ASIC vs FPGA Design Flow, Xilinx FPGA 7 Families
- Vivado Design Suite tool flow
- Demo on Verilog Code to Bitstream generation and FPGA implementation
- Introduction to Zynq-7000 SoC
- Vitis tool flow
- Creating a Simple Embedded Hardware Design
- Extending Hardware System by Adding Peripherals
- Project implementation on FPGA board

Course Fee: INR 10,000/- (Inclusive of tax, Non-refundable)

Program details:
- Classroom sessions from 15th July 2024 to 19th July 2024 at CoreEL Technologies, Bangalore, 10am to 5pm
- Online support on weekly or need basis

Registration link: Click here to register
Last date to register: 12th July 2024

Payment Guidelines:
Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to swathi.s@coreel.com. For assistance, contact Swathi: +91-9686690000.

UPI ID: coreeltechnologiespvtltd@kbl
Current Account No: 0947000104207601
IFSC Code of Bank: KARB0000094

For more details, contact Arun: +91-9844182555 or Swathi: +91-9686690000