FPGA Design using Vivado Design Suite

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India

Dates: 29th Jan – 31st Jan 2025 (Live Online sessions – 10am to 1pm)

Course Description:

This online, live, instructor-led program provides an introduction to digital design tool flow in Xilinx programmable devices using Vivado Design software suite. This course offers introductory training on the Vivado Design Suite and demonstrates the FPGA design flow for those uninitiated to FPGA design. The course provides experience with:

- Creating a Vivado Design Suite project with source files
- Simulating a design
- Performing pin assignments
- Applying basic timing constraints
- Synthesizing and implementing

This course combines lectures with lab exercises to reinforce the concepts.

Who can attend?

- Design Engineers new to Xilinx Vivado
- Engineering graduates aspiring to build a career in VLSI industry as design engineers
- Faculty members and working professionals interested in up-skilling

Pre-requisites:

- Knowledge of digital circuits
- Knowledge of Verilog/VHDL

Course duration:

- 3 days (9 hours – 3 hours per day)

What do I gain?

- Understand the Vivado design flow
- Create and debug HDL designs
- Configure FPGA architecture features, such as Clock Manager, using the Architecture Wizard
- Communicate design timing objectives through the use of Xilinx Design Constraints
- Pinpoint design bottlenecks using the reports
- Utilize synthesis and Implementation options to improve performance
- Create and integrate IP cores into design flow using IP Catalog
- Perform simulation verification
- Floorplanning, I/O Planning using Vivado Design Suite

Course Contents

Day 1

- Introduction to FPGA – FPGA design flow using Xilinx Vivado
- Introduction to FPGA Architecture, SoCs – FPGA families (7 series), Overview of FPGA architecture (CLB, memory and DSP Resources)
- Introduction to Vivado Design Flows
- Elaboration and Simulation – Performing Elaboration and Behavioral simulation for Verilog designs

- Lab 1: Vivado project flow. Generate and download the bitstream to the demo board
- Lab 2: Resources based example design to infer BRAM and DSP slices

Day 2:

- HDL Coding Techniques – Basic digital coding guidelines used in an FPGA design
- Impact of using asynchronous resets in a design
- Synchronous Design Techniques
- Vivado Synthesis and Implementation
- Basics of Static Timing Analysis, calculating Setup and Hold Timing, Setup and hold timing calculations
- Lab 1: Reset methodology
- Lab 2: Design Analysis using Vivado
- Lab 3: Applying basic timing constraints and exploring timing analysis with baseline approach

Day 3:

- Exploring various synthesis and implementation techniques
- Clocking Resources – Various clock resources, clocking layout, and routing in a design
- Creating and Packaging Custom IP - create your own IP and package and include it in the Vivado IP Catalog
- Introduction to Debug Cores (ILA and VIO)
- Lab 1: Usage of VIO in design (block diagram approach)
- Lab 2: ILA Core usage in Instantiation Method in the RTL Code
- Lab 3: ILA Core usage using Netlist Insertion, Mark Attributes, Block Design approach

Course Fee: INR 11,800/- (Inclusive of tax, non-refundable)

Last date for confirmation: 28th Jan 2025

Registration link: Click here to register

For assistance, contact us: +91-6366238254, +91-9686690000