Versal Architecture and Design Methodology

Course dates: 27th Nov to 29th Nov 2024 (10 am to 1 pm IST)

Course Description:

This course is an introduction to AMD Versal Adaptive SoCs in which you will learn the various engines available in the Versal device and also understand the Versal Portfolio. As part of the architectural overview you will be introduced to Scalar Engines, Adaptable Engines, Intelligent Engines and Network on Chip (NoC). We will explore the different AMD tools and flows available for programming AMD Versal Adaptive SoCs and further understand AMD Vitis tool flow. We will also look into the clocking goals of the AMD Versal device and thus describe the clocking architecture.

Who can attend?

- Hardware, Software developers and anyone interested to learn about AMD Xilinx Versal Adaptive SOC

Pre-requisites:

- A basic background of Vivado FPGA Design Flow
- Familiarity with any AMD Device Architecture

Course duration:

- 3 days (9 hours – 3 hours per day)

Key Takeaways:

- Review the architecture of Versal Adaptive SoC
- Describe the different compute resources available in the Versal architecture
- Describe the architectures of the network on chip (NoC) and AI Engine
- Learn about the PMC architecture
- Get an introduction to the Intelligent Engines available in the Versal Adaptive SoC

Course Contents:

Day 1:

- Describes the need for Versal devices and offers an overview of the Versal portfolio
- Provides a high-level overview of the Versal architecture, illustrating the various engines available in the Versal architecture
- Maps the various engines in the Versal architecture to the tools required and describes how to target them for final image assembly
- Describes the software development environments and embedded software development flows for Versal devices. Also introduces embedded software debugging

Day 2:

- Describe the platform management controller (PMC) architecture and interconnects in the AMD Versal™ ACAP
- Describe the primary and secondary boot modes and sources
- Describe the process for generating a boot image
- Exploring Adaptable Engine Architecture of Versal

- Adding IP cores in PL (lab)
- NoC Introduction and Concepts
- Covers the reasons to use the network on chip, its basic elements, and common terminology

Day 3:

- AI Engine: Discusses the AI Engine array architecture, terminology, and AI Engine interfaces
- System Simulation: Explains how to perform system-level simulation in a Versal device design
- DSP Engine: Describe the DSP58 architecture and its features in the AMD Versal™ Adaptive SoC Describe the modes of operation supported by the DSP58 slice
- To create and implement a square root application design using DSP58 primitives. Functional simulation on the implemented design using the AMD Vivado™ simulator

Course Fee: 3 days (9 hours) – Rs. 12,000 (Inclusive of tax, Non-refundable)

Last date for confirmation: 26th Nov 2024

Registration link: Click here to register

For assistance, contact us: +91-9686690000, +91-8754722266