# Design Closure Techniques – STA and Timing Closure in Vivado

**Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD in India**

**Dates: 7th Apr – 21st Jun 2024 (Live Online sessions – 10am to 1pm)**

**Course Description:**
This live, online course helps to review synthesized/implemented database for timing analysis. The program comes with insightful lectures and demos. The emphasis is on utilizing project based flow for navigating the design, creating timing constraints and analyzing timing reports. The course focuses on creating path specific constraints, false paths, max and min delay constraints and priority of the timing exceptions in the Vivado timing engine. The course also addresses on various synthesis and implementation techniques for achieving timing closure.

**Who can attend?**
- FPGA Engineers interested in understanding design closure techniques with respect to timing
- Digital Design engineers interesting in learning about Static Timing Analysis for their designs

**Pre-requisites:**
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

**Course duration:**
- 3 days (9 hours – 3 hours per day)

**What do I gain?**
- Describe setup and hold checks
- Create appropriate clock, input and output delay XDC constraints
- Timing Exceptions
- Analyze different timing reports
- Define a properly constrained design
- Identify key areas to optimize the design to meet performance goals and objectives
- Clock Domain Crossing
- Analyze Clock Domain Crossing Reports
- Synthesis Techniques- Pipelining, Register duplication and Retiming
- Implementation Techniques- Physical optimization and Floor-planning

**Course Contents:**
**Day 1:**
- Introduction to Static Timing Analysis
- Timing Paths - Reg to Reg path, Input to Reg path, Reg to Output paths
- Clock Variations and Uncertainties
- Static Timing Analysis - Setup and Hold check (Equations)
- Analyzing Timing Reports
- Introduction to AMD Design Constraints
- AMD Performance Baselining Flow for Timing Closure

- Lab 1: Baselining Flow: Apply clock constraints, IO Constraints
- Lab 2: Timing Constraints Wizard usage ( to apply clock constraints, IO constraints, virtual clock)

Day 2:

- Multicycle Paths and False Paths /Timing Exceptions
- Lab 1: Lab to demonstrate how to constrain Multicycle paths and False paths
- Synthesis Techniques: Pipelining, resource sharing and register duplication
- Lab 2: Applying Pipelining for improving design performance
- Implementation Techniques : Incremental Compile, Physical Optimization and Floorplanning
- Lab 3: Incremental Compile for improving your design respin time

Day 3:

- Introduction to Floorplanning and Placement blocks (pblocks)
- Lab 1: Floorplanning a complex design using pblocks
- Lab 2: Understand the physical optimization technique for timing closure
- Clock groups and Clock Domain Crossing concepts
- Synchronization Techniques – Addressing Metastability issues using Single bit Metastability resolution circuits and Asynchronous FIFO
- Lab 3: Clock Domain Crossing and Synchronization circuits (Report CDC and apply ASYNC_REG property in your design)

**Course Fee: INR 8,850/- (Inclusive of tax, non-refundable)**

**Last date for confirmation: 6th Apr 2025**

**Registration link:** Click here to register

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