Vivado Advanced Xilinx Design Constraints (XDC) and Static Timing Analysis (STA)

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years

Course date: 30th Jun – 2nd Jul 2021 (10am – 1pm)

Course Description:
This live, online course helps to review the underlying database and static timing analysis (STA) mechanisms. The live, instructor-led program comes with insightful lectures and demos. The emphasis is on utilizing project based scripting flow for navigating the design, creating Xilinx design constraints and analyzing timing reports. The course focuses on creating path specific constraints, false paths, max and min delay constraints and priority of the timing exceptions in the Vivado timing engine. The course also addresses on various synthesis and implementation techniques for achieving better timing closure.

Who can attend?
- FPGA Engineers interested in understanding how to constrain designs for timing
- Digital Design engineers interesting in learning about Static Timing Analysis for their designs

Pre-requisites:
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Course duration:
- 3 days (9 hours – 3 hours per day)

What do I gain?
- Create appropriate clock, input and output delay constraints
- Analyze different timing reports
- Define a properly constrained design
- Describe setup and hold checks
- Identify key areas to optimize the design to meet performance goals and objectives
- Synthesis Techniques- Pipelining and Resource Sharing
- Timing Exceptions
- Implementation Techniques- Incremental compile and Physical optimization
- Congestion and Floorplanning
- Clock domain crossing

Course Contents:
Day 1
- Introduction to Static Timing Analysis – Clock Constraints – Setup and Hold Analysis – Introduction to Baselining- HDL coding techniques
- Lab 1: Clock constraints and I/O constraints
- Use Xilinx recommended synthesis options and techniques to achieve better timing closure
- Lab 2: Resource Sharing, Register Duplication and Pipelining
Day 2:
- Introduction to Timing Exceptions—Pure combinational paths – False and Multicycle paths
- Lab 1: Timing Exceptions
- Build resets into the system for optimum reliability and design speed
- Lab 2: Reset Methodology
- Employing FPGA design best practices and Ultrafast design methodology to improve design speed and reliability
- Lab 3: Incremental Compile

Day 3:
- Identifying Congestion and addressing congestion issues – Use Physical optimization techniques for timing closure
- Lab 1: Physical Optimization
- Introduction to Floorplanning and how to use Pblocks while floorplanning – FloorplanningGuidelines – Achieving Timing Closure
- Lab 2: Floorplanning
- Virtual clocks – clock groups – physically exclusive, logically exclusive and asynchronous clocks
- Lab 3: Clock domain crossing
- Design Closure – UltraFast Design Methodology Guidelines

Course Fee: 3 days (9 hours) – Rs. 2,499 (Inclusive of tax)

Last date for confirmation: 29-Jun-2021

Registration link: Click here to register

Payment Guidelines:
Participants of Sandeepani training modules can make the course fee payment through online transfer via your Google Pay/PhonePe/Internet Banking Account to the following account and proof of the same to be scanned & mailed to xtc@coreel.com.

UPI ID: coreeltechnologiespvtltd@kbl
Current Account No: 0947000104207601
IFSC Code of Bank: KARB0000094

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