Embedded System Design using Zynq UltraScale+ MPSoC

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India

Course dates: 19th Feb – 21st Feb 2025 (10am-1pm)

Course Description:

This course provides hardware designers with an overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a hardware architectural perspective. The emphasis is on:

- Identifying the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- Illustrating the processing system (PS) and programmable logic (PL) connectivity
- Utilizing QEMU to emulate hardware behavior

Who can attend?

- Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ MPSoC device
- Students pursuing BE/BTech/ME/MTech/Research who intend learning about or using Zynq UltraScale+ MPSoC device for project work/research

Pre-requisites:

- Suggested: Understanding of the Zynq-7000 architecture
- Basic familiarity with embedded software development using C (to support testing of specific architectural elements)

Course duration:

- 3 days (9 hours – 3 hours per day)

What do I gain?

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- List the various power domains and how they are controlled
- Describe the connectivity between the Processing System (PS) and Programmable Logic (PL)
- Utilize QEMU to emulate hardware behavior

Course Contents:

Day 1

- Zynq UltraScale+ MPSoC Application Processing Unit: Introduction to the members of the APU, Cortex™-A53 processor and how the cluster is configured and managed
- HW-SW Virtualization: Covers the hardware and software elements of virtualization
- Real-Time Processing Unit: Focuses on the real-time processing module (RPU) in the PS
- Lab 1: APU Architecture Extensions NEON
- Lab 2: Creating a bare-metal application that targets the RPU

Day 2

- QEMU: Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available

- Booting: How to implement the embedded system, including the boot process and boot image creation
- First Stage Boot Loader: Demonstrates the process of developing, customizing, and debugging this mandatory piece of code
- System Protection: Covers all the hardware elements that support the separation of software domains
- Lab 3: QEMU Bare-Metal Application Development and Debugging
- Lab 4: Boot and Configuration

Day 3

- Clocks and Resets: Overview of clocking and reset, focusing more on capabilities than specific implementations
- AXI: Understanding how the PS and PL connect enables designers to create more efficient systems
- Power Management: Overview of the PMU and the power-saving features of the device
- Lab 5: Exploring AXI Transactions Using the AXI Traffic Generator
- Lab 6: Zynq MPSoC PS-PL demo

Course Fee: 3 days (9 hours) – Rs. 14,160 (Inclusive of tax, Non-refundable)

Last date for confirmation: 18th Feb 2025

Registration link: Click here to register

For assistance, contact us: +91-6366238254, +91-9686690000