



Online On-demand – FPGA Architecture – Xilinx UltraScale and UltraScale+

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India

Course Description:

This self-paced online course gives participants an in-depth view of the UltraScale and UltraScale+ FPGA Architecture from Xilinx. It covers the various logic, memory, DSP, clocking and I/O resources available on the UltraScale and UltraScale+ family of Xilinx devices. The program comes with insightful theory lectures, lab code and lab demos.

Who can attend?

- Engineers who are new to FPGA technology
- Faculty, Research Scholars and students who need to understand FPGA Architecture for their research or project work

Pre-requisites:

- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Access:

- Login and password will be shared within 1 business day after payment and registration
- Content will be made available for 1 month from start of access

Software Tools:

Xilinx Vivado

What do I gain?

- Get a broad overview of typical FPGA architecture
- Understand available resources on Xilinx UltraScale and UltraScale+ FPGA devices
- Learn how various logic, memory, DSP, clocking and I/O resources can be utilized

Course Contents:

- Chapter 1 Introduction to FPGA Families
 - Video lecture Introduction to FPGA Families
- Chapter 2 CLB Resources
 - Video lecture 7-Series CLB Resources
 - Lab demo 7-Series CLB Resources
 - Video lecture UltraScale CLB Resources
 - o Lab demo UltraScale CLB Resources
 - Video lecture HDL Coding Techniques
 - o Lab demo HDL Coding Techniques
- Chapter 3 Memory Resources
 - Video lecture 7-Series LUT as memory and shift register
 - Lab demo 7-Series LUT as memory and shift register
 - Lab demo UltraScale CLB as shift register
 - Video lecture 7-Series BRAM Resources
 - Lab demo 7-Series BRAM Resources
 - o Lab demo UltraScale BRAM Resources





- o Lab demo UltraScale Distributed RAM Resources
- Video lecture URAM Resources
- o Lab demo URAM Resources
- Chapter 4 DSP Resources
 - Video lecture Comparison of 7 Series and UltraScale DSP Resources
 - o Lab demo 7 Series and UltraScale DSP Resources
- Chapter 5 Clocking Resources
 - Video lecture 7-Series Clocking Resources
 - Lab demo 7-Series Clocking Resources
 - o Video lecture UltraScale Clocking Resources
 - Lab demo UltraScale Clocking Resources
- Chapter 6 Design Migration Techniques
 - Video lecture Design Migration Techniques
 - o Lab demo Design Migration Techniques

Course Fee: INR 6,999/- (Inclusive of tax. Course fee is non-refundable)

Registration link: Click here to register

Payment Guidelines:

Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to training@coreel.com. For assistance, contact us: +91-9844182555, +91-9686690000.

UPI ID: coreeltechnologiespvtltd@kbl Current Account No: 0947000104207601 IFSC Code of Bank: KARB0000094



