# Accelerating Applications with the Vitis Unified Software Environment

**Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years**

**Course Description:**

In this interactive online workshop, you will learn how to develop, debug, and profile new or existing C/C++ and RTL applications in the Vitis™ unified software environment targeting both data center (DC) and embedded applications. The emphasis of this course is on:

- Building a software application using the OpenCL API and the Linux-based Xilinx runtime (XRT) to schedule the hardware kernels and control data movement on an embedded processor platform
- Demonstrating the Vitis environment GUI flow and makefile flow for embedded applications
- Describing the Vitis platform execution model and XRT
- Describing kernel development using C/C++ and RTL
- Utilizing the Vitis analyzer tool to analyze reports
- Explaining the design methodology to optimize a design

**Who can attend?**

- Anyone who needs to accelerate their software applications using FPGAs, SoCs (such as Zynq®-7000 SoCs, Zynq UltraScale+™ MPSoCs), and Versal™ ACAPs

**Pre-requisites:**

- Basic knowledge of Xilinx FPGA architecture
- Comfort with the C/C++ programming language
- Software development flow

**Course Duration**

- 3 days (9 Hours – 3 hours per day)

**Software Tools:**

Vitis unified software environment 2019.2. This course combines lectures with lab exercises to reinforce the concepts.

**What do I gain?**

After completing this comprehensive training, you will have the necessary skills to:

- Describe how the FPGA architecture lends itself to parallel computing
- Explain how the Vitis unified software environment helps software developers to focus on applications
- Describe the Vitis (OpenCL API) execution model
- Analyze the OpenCL API memory model
- Create kernels from C, C++, or RTL IP using the RTL Kernel Wizard
- Apply host code optimization and kernel optimization techniques
- Move data efficiently between kernel and global memory
- Profile the design using the Vitis analyzer tool

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**Course Contents**

**Day 1:**

- Introduction to the Vitis Unified Software Platform – Explains how software/hardware engineers and application developers can benefit from the Vitis unified software environment and OpenCL framework. {Lecture}
- Vitis IDE Tool Overview – Describes the elements of the development flow, such as software emulation, hardware emulation, and system run as well as debugging support for the host code and kernel code. {Lecture, Lab}
- Vitis Command Line Flow – Introduces the Vitis environment makefile flow where the user manages the compilation of host code and kernels. {Lecture, Lab}
- Introduction to Hardware Acceleration – Outlines the fundamental aspects of FPGAs, SoCs, and ACAPs that are required to guide the Vitis tool to the best computational architecture for any algorithm. {Lecture}

**Day 2:**

- Alveo Data Center Accelerator Cards Overview – Describes the Alveo Data Center accelerator cards and lists the advantages of these cards and the available software solutions stack. {Lecture}
- Alveo Accelerator Card Ecosystem Partner Solutions Overview – Outlines the partner solutions available in the cloud and on premises for Alveo Data Center accelerator cards. {Lecture}
- Vitis Execution Model and XRT Describes the XRT and the OpenCL APIs used for such as setting up the platform, executing the target device and post-processing. {Lecture, Lab}
- Lab: This lab introduces you to the common structure of an OpenCL™ framework application.

**Day 3:**

- Synchronization – Describes OpenCL synchronization techniques such as events, barriers, blocking write/read, and the benefit of using out-of-order execution. {Lecture, Lab}
- Introduction to C/C++ based Kernels – Describes the trade-offs between C/C++, OpenCL, and RTL applications and the benefits of C-based kernels. {Lecture, Lab}
- Using the RTL Kernel Wizard to Reuse Existing IP as Accelerators – Describes how the Vitis unified software development provides RTL kernel developers with a framework to integrate their hardware functions into an application running on a host PC connected to an FPGA via a PCIe® interface.

**Registration link:** Click here to register