Designing with Versal ACAP

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years

Course Description:

This course provides an overview of the hard block capabilities for the Versal ACAP
The focus is on:

- Describe the Versal™ ACAP architecture at a high level
- Describe the various engines in the Versal ACP device
- Use the various blocks from the Versal architecture to create complex systems

Who can attend?

- Hardware designers having knowledge on architecture and capabilities of the UltraScale and UltraScale+ and Zynq UltraScale + and Vitis

Pre-requisites:

- Comfort with the C/C++ programming language
- Vitis IDE software development flow
- Hardware development flow with the Vivado Design Suite
- Basic knowledge of UltraScale™/UltraScale+™ FPGAs and Zynq® UltraScale+ MPSoC

Course Duration

- 3 days (9 Hours – 3 hours per day)

What do I gain?

- Describe in general the new Versal ACAP
- Identify typical applications of Versal ACAP
- Booting and its concepts
- Versal ACAP and Vitis flow

Course Contents

Day 1:

- Introduction
- Architecture Overview
- Design Tool Flow

Day 2:

- Adaptable Engines (PL)
- Processing System
- PMC and Boot and Configuration

Day 3:

- SelectIO Resources
- Clocking Architecture
- System Interrupts

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