Ultrafast Design Methodology using Xilinx Vivado

Sandeepani is a training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years

Course Description:
This online, live, instructor-led program describes ultrafast design methodology checklist. The course describes the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with Ultrafast™ design methodology case studies. The course combines lectures with lab exercises to reinforce the concepts.

Who can attend?
- Post graduate students interested in gaining knowledge on Timing Closure techniques
- Faculties
- Professionals from DEFENCE / CORPORATE / INDUSTRY

Pre-requisites:
- Basic knowledge in HDL (VHDL/Verilog)

Course Duration
- 3 days (9Hours – 3 hours per day)

What do I gain?
- Optimize HDL code to maximize the FPGA resources
- Define a properly constrained design
- Project based and Non Project batch scripting
- Essential Tcl Scripting for the Vivado Design Suite
- Synchronous design techniques
- Handling multiple clocks
- Timing closure techniques and Last mile strategies

Course Contents
Day 1:
- Introduction to Ultrafast design methodology-Device Planning and Design Creation
- Lab 1: Synchronous design techniques
- HDL Coding Techniques – Synthesis and Implementation Guidelines
- Lab 2: Project and Non Project batch Scripting Flow
- Designing with the IP Integrator
- Lab 3: Creating and Packaging custom IP

Day 2:
- Introduction to Tcl Scripting
- Lab 1: Extracting Logic Levels using Tcl

- Ultrafast Design Methodology – Design Closure
- Lab 2: Physical Optimization
- Synchronization Circuits- Achieving Effective Timing Closure
- Lab 3: Timing Closure

Day 3:

- Handling Multiple clocks – Clock domain crossing techniques
- Lab 1: Generated clocks and clock group constraints
- Routing Congestion- Post Placement and Post route optimization techniques
- Lab 2: Floorplanning
- Ultrafast design methodology guidelines
- Lab 3: Effective Migration techniques with timing closure

Registration link: Click here to register