Online On-demand – RTL Modeling using SystemVerilog

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India

Course Description:
This self-paced course introduces the SystemVerilog language and its enhancements over Verilog, viz., data types, structures, arrays, procedural blocks, enhanced procedural constructs, reusable tasks and packages. The program comes with insightful theory lectures, lab code and lab demos.

Who can attend?
- Undergraduate and post-graduate students interested in up-skilling
- Faculty members, FPGA designers and RTL Design engineers

Pre-requisites:
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Access:
- Login and password will be shared within 1 business day after payment and registration
- Content will be made available for 1 month from start of access

Software Tools:
- Any simulator, such as QuestaSim and Vivado. Demos are on QuestaSim

What do I gain?
- Describe the benefits and features of SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type
- Explain how to use arrays, structures and unions for RTL coding
- Describe the new procedural blocks and their effect on Synthesis
- Define the ability to reuse tasks and packages

Course Contents:
- Chapter 1 – Introduction to SystemVerilog
  - Video lecture: Introduction to SystemVerilog
  - Lab demo: Simulating a SystemVerilog design using QuestaSim
- Chapter 2 – SystemVerilog Data types and operators
  - Video lecture: Data types and operators
  - Lab demo: Logic data type
  - Lab demo: Operators
- Chapter 3 – SystemVerilog Associations
  - Video Lecture: Port Associations
- Chapter 4 - SystemVerilog Procedural blocks and routines
  - Video Lecture: Procedural blocks and routines
  - Lab demo: Specialized always blocks
- Chapter 5 – SystemVerilog Enumerated data types
  - Video lecture: Enumerated data types

- Chapter 6 – Arrays, Structures, Unions and Packages
    - Video Lecture: Arrays, Structures, Unions and Packages
    - Lab demo: Packed and unpacked arrays
    - Lab demo: Structures and string operations
- Chapter 7 – SystemVerilog Interfaces
    - Video Lecture: Interfaces

Course Fee: INR 4,999/- (Non-refundable, Inclusive of tax)

Registration link: Click here to register

Payment Guidelines:
Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to training@coreel.com. For assistance, contact us: +91-9844182555, +91-9686690000.

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