

Online On-demand – Physical Verification using Calibre

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India

Course Description:

This self-paced course provides a detailed description of the ASIC Physical Verification process. The program comes with theory lectures, lab demos and hands-on labs on a cloud environment. Some of the key concepts covered are DRC, LVS and Parasitic Extraction.

Who should attend?

- ASIC Design Engineers, Full-custom and Semi-custom Design Engineers interested in moving into Physical Verification domain
- Academicians and students eager to build a career as ASIC Physical Design Engineer

Pre-requisites:

- CMOS concepts
- Comfortable with schematic design and layout design

Access:

- Login and password will be shared within 1 business day after payment and registration
- Content will be made available for 1 month from the date of sharing login and password to access content
- Lab access time is included in this 1 month
- Credentials to access cloud machine for hands-on lab will be shared prior to start of labs

What do I gain?

After completing this comprehensive training, you will:

- Get an introduction to the IC Design flow
- Understand Physical Verification and how it fits into the chip design flow
- Learn about Design Rule Checks (DRC), Layout vs Schematic (LVS) and Parasitic Extraction (PEX)
- Get a practical insight through lab demonstrations
- Perform hands-on labs on a cloud environment

Course Contents

- Introduction to IC design flows
 - Video lecture 1 – Introduction to IC design flows
- Introduction to Physical Verification
 - Video lecture 2 – Introduction to Physical Verification
- Basic DRC Concepts
 - Video lecture 3 – Basic DRC Concepts – Block level
 - Demo 1 – Block level DRC checks
- Advanced DRC Concepts
 - Video lecture 4 – Advanced DRC Concepts – Chip level
 - Demo 2 – Chip level DRC checks
 - Demo 3 – Chip level DRC checks

- Hands-on Lab 1
 - Lab 1 – Schematic editing using sedit
 - Lab 2 – Layout editing using ledit
 - Lab 3 – DRC checks using calibre
- Introduction to LVS
 - Video lecture 5 – Introduction to LVS
- LVS Text based Connectivity Checks, Soft Connection errors and Fixing Methodologies
 - Video lecture 6 – LVS Text based Connectivity Checks, Soft Connection errors and Fixing Methodologies
 - Demo 4 – LVS Text based Connectivity Checks, Soft Connection errors and Fixing Methodologies
 - Demo 5 – LVS Text based Connectivity Checks, Soft Connection errors and Fixing Methodologies
- LVS Shorts and Open circuit errors and Fixing Methodologies
 - Video lecture 7 – LVS Shorts and Open circuit errors and Fixing Methodologies
 - Demo 6 – LVS Shorts and Open circuit errors and Fixing Methodologies
 - Demo 7 – LVS Shorts and Open circuit errors and Fixing Methodologies
 - Demo 8 – LVS Shorts and Open circuit errors and Fixing Methodologies
- Hands-on Lab 2
 - Lab 4 – LVS open circuit check
 - Lab 5 – LVS short circuit check
 - Lab 6 – LVS port name check
 - Lab 7 – LVS malformed device
- Introduction to Parasitic Extraction and PEX Concepts
 - Video lecture 8 – Introduction to Parasitic Extraction and PEX Concepts
 - Demo 9 – Various Parasitic Models and Extraction Methods
- Hands-on Lab 3
 - Lab Instructions 3
 - Lab 8 – Parasitic extraction

Demo video: <https://sandeepani-training.com/elearn/lesson/pv-calibre-ch1>

Course Fee: INR 5,999/- (Inclusive of tax. Course fee is non-refundable)

Registration link: [Click here to register](#)

Payment Guidelines:

Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to training@coreel.com. For assistance, contact us: +91-9844182555, +91-9686690000.

UPI ID: coreeltechnologiespvtltd@kbl
Current Account No: 0947000104207601
IFSC Code of Bank: KARB0000094

BHIM UPI PAYMENT ACCEPTED
SCAN QR CODE TO PAY

