Zynq UltraScale+ MPSoC for the Hardware Designer

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years

Course Description:
This course provides hardware designers with an overview of thecapabilities and support for the Zynq® UltraScale+™ MPSoC familyfrom a hardware architectural perspective.
The emphasis is on:

- Identifying the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- Reviewing the various power domains and their control structure
- Illustrating the processing system (PS) and programmable logic (PL) connectivity
- Utilizing QEMU to emulate hardware behavior

Who can attend?

- Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ MPSoC device

Pre-requisites:

- Suggested: Understanding of the Zynq-7000 architecture
- Basic familiarity with embedded software development using C (to support testing of specific architectural elements)

Software Tools:

- Vivado Design Suite
- Vitis unified software platform
- Hardware emulation environment: QEMU
- Ubuntu desktop
- PetaLinux

Hardware

- Zynq UltraScale+ MPSoC ZCU104 board

Course duration:

- 3 days (9 hours – 3 hours per day)

What do I gain?

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- List the various power domains and how they are controlled
- Describe the connectivity between the processing system (PS) and programmable logic (PL)
- Utilize QEMU to emulate hardware behavior

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Course Contents:

Day 1

- Application Processing Unit: Introduction to the members of the APU, specifically the Cortex™-A53 processor and how the cluster is configured and managed.
- HW-SW Virtualization: Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used.
- Real-Time Processing Unit: Focuses on the real-time processing module (RPU) in the PS, which is comprised of a pair of Cortex processors and supporting elements.
- Lab 1: APU Architecture Extensions NEON
- Lab 2: Hardware-Software Virtualization Using a Hypervisor

Day 2

- QEMU: Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available.
- Booting: How to implement the embedded system, including the boot process and boot image creation.
- First Stage Boot Loader: Demonstrates the process of developing, customizing, and debugging this mandatory piece of code.
- Lab 3:QEMU Bare-Metal Application Development and Debugging
- Lab 4: RPU Introduction

Day 3

- Video: Introduction to video, video codecs, and the video codec unitavailable in the Zynq UltraScale MPSoC.
- System Protection: Covers all the hardware elements that support the separation of software domains.
- Clocks and Resets: Overview of clocking and reset, focusing more on capabilitiesthan specific implementations.
- AXI Understanding how the PS and PL connect enables designers to create more efficient systems.
- Power Management Overview of the PMU and the power-saving features of the device.
- Lab 5: Boot and Configuration
- Lab 6:Exploring AXI Transactions Using the AXI Traffic Generator

Registration link: Click here to register

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