Online Internship on Functional Verification using SystemVerilog

(Live Online sessions – 1 hour/day, Mon to Fri)

Description:
Sandeepani offers 1 month Online Internship Program for students currently doing their B.E/B.Tech,M.E./M.Tech in Electronics/Instrumentation/Electrical/Telecommunication. This program is specifically designed to introduce participants to functional verification using the SystemVerilog HVL. The participants will get an opportunity to work on a project during the course.

Program Highlights

- 24/7 access to Mentor Graphics licenses
- Conceptual training on topics outside regular university curriculum
- Hands-on labs using industry standard EDA tools from Mentor Graphics
- Live, online classes for 1 hour/day – 6pm to 7pm

Duration: -

- 4 weeks (20 Hours) – (Daily 1 hour: 6pm to 7pm)

Eligibility criteria:

- Pursuing B.E/B.Tech in Electronics and Communication/Instrumentation/Telecommunication/Electrical Engineering
- Pursuing M.E./M.Tech/Research Scholar in VLSI and Embedded System Design
- Faculty members keen on learning Design Verification using SystemVerilog
- Working professionals interested in skill development

Pre-requisites:

- Basics of Digital
- Basic Understanding of Verilog

Key takeaways:

- Describe the advantages and enhancements to SystemVerilog to support verification
- Define the new data types available in SystemVerilog
- Analyze and use the improvements to tasks and functions
- Discuss and use the various new verification building blocks available in SystemVerilog
- Describe object-oriented programming and create a class-based verification environment
- Explain the various methods for creating random data
- Create and utilize random data for generating stimulus to a DUT
- Identify how SystemVerilog enhances functional coverage for simulation verification
- Utilize assertions to quickly identify correct behavior in simulation

Tools:

- Mentor Graphics QuestaSim **(24/7 Trial license access will be provided for the duration of the Internship)**

Course Content:

WEEK 1: (5 HRS, 1Hr /Day)

Theory:

- Introduction to verification and Various Components of Verification Environment.
- System Verilog Data types (logic, bit, byte, longint, shortint, arrays, associative, dynamic and queues)
- SV Procedural Blocks and routines (Specialized Procedural blocks, always blocks, final, unique and priority, continue and break, fork join_any, none, foreach, tasks and functions, packages)

LAB:

- Defining System Verilog DataTypes
- Writing Procedural Blocks, Procedural statements and Flow Control.

WEEK 2: (5Hrs, 1Hr /Day)

Theory:

- System Verilog OOP (Classes, objects, Inheritance, Polymorphism, static, automatic, local, protected)
- Interfaces, Virtual Interfaces, Parameterized Interfaces, SV tasks and functions within interfaces) and Clocking Blocks.
- Randomization (randomize, pre randomize and post randomize, randcase, std:: randomize, rand)
- Threads and Inter-process Communication (Mailboxes, Semaphores)

LAB:

- Defining Class and implement the OOPs concepts on it
- Defining Interfaces for a design
- Generation of transaction class with Randomization and using constraints
- Adding mailbox to the code to understand the Concept of IPC in language

WEEK 3: (5 Hrs, 1hr/Day)

Theory:

- System Verilog Assertions (Immediate and Concurrent Assertions)
- Program and SV Enhanced Regions
- System Verilog Coverage (Introduction, Code and Functional Coverage, coverage types, functional coverage strategies, simple functional coverage example, cover group, coverage options, analyzing coverage data, measuring coverage statistics during simulation)

LAB:

- Implementing Assertions for an FSM Code and verifying its functionality with QuestaSim
- Defining Coverage with help of Cover groups and Cover point and analyzing results using QuestaSim

WEEK 4: (5 Hrs, 1hr/day)

PROJECT WORK:

- Development of Verification environment (Generator, Driver, Monitor and Scoreboard) for a digital Design from scratch, and getting verifying the functionality of design using the same

Course Fee: 1 month (1 hour/day) – INR 4,000/- (Inclusive of tax)

Registration link: Click here to register

For more information, contact Swathi: +91-9686690000.