Internship on Physical Design and Verification - RTL2GDSII

Description:
Sandeepani offers 1 month Online Internship Program for students currently doing their B.E/B.Tech,M.E./M.Tech in Electronics/Instrumentation/Electrical/Telecommunication. This program is designed to introduce participants to the semi-custom RTL to GDSII flow in ASIC Physical Design. The participants will get an opportunity to work on a project during the course.

Program Highlights

- 24/7 access to Mentor Graphics licenses
- Conceptual training on topics outside regular university curriculum
- Hands-on labs using industry standard EDA tools from Mentor Graphics
- Live, online classes for 1 hour/day – 5pm to 6pm

Duration:

- 4 weeks (20 Hours) – (Daily 1 hours)

Who can attend?

- Undergraduate students in III or Final year of Engineering
- Post graduate students interested in gaining knowledge in Analog domain

Pre-requisites:

- Basic understanding of Digital Circuits and Verilog

Key takeaways:

- Understand the Semi-custom ASIC Physical Design flow from RTL to GDSII
- Learn about the inputs required for synthesis and different synthesis techniques
- Understand the relevance of Clock Tree Synthesis and Static Timing Analysis
- Learn Place and Route techniques
- Apply physical verification rules like DRC and LVS

Tools:

- Mentor Graphics tools for simulation, synthesis, physical design and physical verification **(24/7 Trial license access will be provided for the duration of the Internship)**

Course Content:

WEEK 1:

- Introduction to Semi Custom Design flow, basic Linux commands and basic Verilog
- RTL Design entry and simulation
- Introduction to Synthesis – Inputs and Outputs, File formats
- Assignment: Simulation of combinational and sequential circuits

WEEK 2:

- Synthesis Techniques
- Physical Synthesis and Logical Synthesis
- Clocks and timing Checks
- Static Power, Dynamic Power, Switching Activity & Leakage Currents Reports
- Post Synthesis Simulation
- Assignment: Synthesis of logic blocks

WEEK 3:

- Physical Placement & Signal Routing
- Power & optimization Techniques
- Graphic Design Stream (GDS II) - Generation
- Physical Layout verification Methodologies using Calibre Tool
- Design Rule Checks – DRC
- Assignment: PNR of logic blocks

WEEK 4:

PROJECT WORK:

- Design Rule Checks – LVS
- Parasitic Extraction – PEX
- Additional DRC and LVS Options in Calibre tool
- Exporting to GDSII stream and Verify
- Demonstration of RTL2GDSII flow for complex designs
    - CPU design
    - Memory designs
- Project Assignments

Registration link: Click here to register