Online Internship on Full Custom ASIC Design and Verification

Description:
This online, live, instructor-led Internship program provides an Introduction to ASIC Design and Verification Environment. It addresses the full custom design flow strategies to verify designs using Industry standard Mentor Graphics EDA tools. Some of the topics addressed include Design challenges & Optimization techniques in transistor model, various Analyses on transistor model like transient, DC and AC analysis, Post Layout simulation environment, issues of Place and Route in full custom designs and Physical Verification strategies using signoff Calibre tool for various Layout checks - DRC, LVS and PEX rule files.

Program Highlights
- 24/7 access to Mentor Graphics licenses
- Conceptual training on topics outside regular university curriculum
- Hands-on labs using industry standard EDA tools from Mentor Graphics
- Live, online classes for 1 hour/day – 5pm to 6pm

Duration:
- 4 weeks (20 Hours) – (Daily 1 hour: 5pm to 6pm)

Who can attend?
- Undergraduate students in III or Final year of Engineering
- Post graduate students interested in gaining knowledge in Analog domain

Pre-requisites:
- Basics of Analog and Digital circuit designs
- Basics of Transistor Models
- Basics of Lambda based rules for Verification
- Stick diagram, Layout basics

What do I gain?
- Full custom design flow
- MOS switches and design
- Transistor model -full custom design - Analysis, Power, area optimizations
- VI Characteristics of MOS, Transmission Gates
- MOSFET Combinational and sequential logic
- Aspects of Physical Layout model and Its Challenges
- SPICE Generation, Analysis and post layout simulations
- Physical Verification Aspects

Tools:
- ➢ Mentor Graphics tools for design entry, simulation, analysis and physical verification **(24/7 Trial license access will be provided for the duration of the Internship)**

Course Contents

Week 1:
- Overview of ASIC vs FPGAs
- Full Custom Flow and Semi Custom Design Flow
- Introduction to Full Custom Design Tools
- Schematic Entry, Spice Models, Simulation
- DC, AC and Transient Analysis
- Transient and Power Analysis
- Labs: Inverter, Transmission Gates, NAND/NOR Gates
- Assignment

Week 2:
- Introduction to Mixed Design and Analog designs
- Design Entry - Transistor Modeling
- SPICE Analysis and Simulation
- Reports of power, area calculations and Optimization techniques
- DC, AC and Transient Analysis and Power Analysis
- Labs: Common Source Amplifier, Differential amplifier, D-FF/Latch, Op-Amplifier
- Assignment

Week 3:
- Introduction to ASIC Physical Layout
- CMOS Fabrication Overview and the Design Rules
- Aspects of Physical Layout and Its Challenges
- Floor planning, Placement, Routing
- Physical Verification Using Calibre Tool (DRC, LVS, xRC)
- Post layout simulation /Back annotation using ELDO/T-spice Simulator
- Labs: Layout entry for Transmission Gate, Operation Amplifier
- Assignment

Week 4:
- Circuit Optimization Techniques
- Complex Designs (Sigma Delta Designs and their Subset Blocks)
- ADC and DAC Challenges and their Physical Design & Implementations
- Design Entry - Transistor Modeling
- SPICE Analysis and Simulation
- Reports of power, area calculations and Optimization techniques
- DC, AC and Transient Analysis and Power Analysis
- Labs: Voltage Controlled Oscillator, NAND/NOR Gates
- Assignment

Registration link: Click here to register