

## High-Level Synthesis with the Vitis HLS Tool

**Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years**

### Course Description:

The course provides a thorough introduction to the Vitis High-Level Synthesis (HLS) tool. This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. It also describes how to utilize the Vitis HLS tool to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

### Who can attend?

- Software and hardware engineers looking to utilize high-level synthesis in their designs

### Pre-requisites:

- Knowledge of C, C++ or System C

### Course duration:

- 3 days (9 hours – 3 hours per day)

### What do I gain?

- Enhance productivity using the Vitis HLS tool
- Describe the high-level synthesis flow
- Use the Vitis HLS tool for a first project
- Identify the importance of the test bench
- Use directives to improve performance and area and select RTL interfaces
- Identify common coding pitfalls as well as methods for improving code for RTL/hardware

### Course Contents:

#### Day 1

- Introduction to High-Level Synthesis
- Basics of the Vivado HLS Tool and the Vitis HLS Tool
- Lab1:Vitis HLS Tool Flow
- Design Exploration with Directives
- Vitis HLS Tool Command Line Interface
- Lab2: Vitis HLS Tool Command Line Interface flow
- Introduction to I/O Interfaces
- Block-Level Protocols
- Lab3 : Block-Level I/O Protocols

#### Day 2

- Port-Level I/O Protocols
- Lab4: Port-Level I/O Protocols: Memory Interface
- Pipeline for Performance: PIPELINE
- Lab5: Pipeline for Performance: PIPELINE
- Optimizing Structures for Performance
- Lab6: Optimizing Structures for Performance

- Data Pack and Data Dependencies
- Vitis HLS Tool Default Behavior: Latency

### Day 3

- Improving Area
- Lab7: Improving Area and Resource Utilization
- Introduction to HLx Design Flow
- Lab8: HLx Design Flow – System Integration
- Vitis HLS Tool C Libraries: Arbitrary Precision
- Lab9: Vitis HLS Tool C Libraries Arbitrary Precision

Registration link: [Click here to register](#)