# Online On-demand – Embedded System Design using Zynq

**Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India**

**Course Description:**
This self-paced online course gives participants an in-depth view of the Embedded System Design flow using Xilinx tools and technologies. It covers the Zynq-7000 architecture, PS-PL interface, using the IP Integrator in Vivado and Software flow and Debugging using Vitis. The program comes with insightful theory lectures, lab code and lab demos.

**Who can attend?**
- Design Engineers and Firmware Engineers interested to learn about Xilinx SoC flow using Vivado and Vitis
- Students pursuing BE/BTech/ME/MTech/Research who intend learning about or using FPGAs/SoCs for project work/research

**Pre-requisites:**
- Knowledge of Digital Circuits and Verilog HDL
- Basic understanding of FPGA
- Basic Knowledge of C programming
- Basic Microprocessor experience

**Access:**
- Login and password will be shared within 1 business day after payment and registration
- Content will be made available for 1 month from start of access

**Software Tools:**
- AMD-Xilinx Vivado
- AMD-Xilinx Vitis

**What do I gain?**
- Explore various features of Zynq SoC for Hardware-Software co-design
- Understand the AXI Interconnect Standard and its variations
- Learn the Embedded System Design Flow using AMD-Xilinx Vitis
- Extend the hardware system with Xilinx provided peripherals
- Write a software application to access peripherals
- Work with Processing System Timers
- Learn about Software Debugging
- Analyze system performance using Profiling Tool

**Course Contents:**
- Chapter 1 – Introduction to Embedded System Design
  - Video lecture
- Chapter 2 –AMD- Xilinx SoC Design Flow
  - Video lecture – Overview of Embedded Hardware Development
  - Video lecture – Overview of Embedded Software Development
  - Video lecture – Driving the Vitis Software Development Tool
  - Lab demo – Simple Hardware Design

- Chapter 3 – Zynq Architecture
    - Video lecture – Application Processor Unit (APU)
    - Video lecture – Input/Output Peripherals
    - Lab demo – PS-UART
- Chapter 4 – PS-PL Interface
    - Video lecture – PS-PL Interface
    - Video lecture – AXI-Introduction
    - Video lecture – AXI-Variations
    - Video lecture – AXI-Transactions
    - Lab demo – Adding Peripherals in Programmable Logic
- Chapter 5 – IP Integrator and Packager
    - Video lecture – Designing with IP integrator
    - Video lecture – Creating a custom IP
    - Lab demo – Creating and Adding Your Own Custom IP (AXI IP)
- Chapter 6 – Debugging
    - Video lecture – Debugging the Zynq SoC
    - Lab demo – Working with Timers and Debugging Applications using Vitis
- Chapter 7 – Introduction to MPSoC and RFSoC architectures
    - Video lecture – Introduction to MPSoC and RFSoC architectures

**Demo video:** https://sandeepani-training.com/elearn/lesson/introduction-to-embedded-system-design

**Course Fee: INR 6,999/- (Inclusive of tax. Course fee is non-refundable)**

**Registration link:** Click here to register

**Payment Guidelines:**
Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to training@coreel.com. For assistance, contact us: +91-9844182555, +91-9686690000.

UPI ID: coreeltechnologiespvtltd@kbl
Current Account No: 0947000104207601
IFSC Code of Bank: KARB0000094